

VLSI-Based Electronic Voting Machine

M. Raja Kumar¹, B. Anitha², R. Pravallika³, D. K. Kavitha⁴, S. Joseph⁵, N. Rambabu⁶, and R. GopiNaik⁷

^{1,2}Assistant Professor, Department of Electronics and Communication Engineering, PACE Institute of Technology and Sciences, Ongole, Andhra Pradesh, India

^{3,4}UG Student, Department of Electronics and Communication Engineering, PACE Institute of Technology and Sciences, Ongole, Andhra Pradesh, India

^{5,6,7}Assistant Professor, Department of Electrical and Electronics Engineering, PACE Institute of Technology and Sciences, Ongole, Andhra Pradesh, India

Correspondence should be addressed to M. Raja Kumar; rajakumar_m@pace.ac.in

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ABSTRACT- Voting in the paper was a time-consuming and erroneous process. Voting by electronic voting machine (EVM) is a simple, secure, and time-saving technology. The proposed paper consists of the parties assigned to the election can be represented in the box along with the total number of contestants participating in the election process. Ahdar Biometric is also included in the machine which is a key role paid to avoid fraudulent voters and to prevent fraud. In the voting process begins when a voter votes for a particular party through the adhar bio metric process after the buzzer will display a notification of who voted for the party displayed on the screen. After the completion of the voting process the votes are confirmed by comparing the votes cast with the contestants in their respective The proposed method is usefull for college level to all election boards and digital voting system for real-time applications ranging from community college elections to university level elections, as it has the advantage of being able to be re-programmed to perform different functions according to the user's wishes, which helps to reduce prevalence. expenditures.

KEYWORDS- VHDL, FPGA LCD Display, Adhar Bio metric, Voting Machine

I. INTRODUCTION

In any vote-based system, casting a ballot is the sole criteria for citizens to choose their representatives. As a result, this entire method should be carried out with the utmost care so that only a reasonable and deserving candidate is chosen solely on the basis of popular vote. Previously, judgments were made using a poll paper structure, in which people cast their votes for their favourite challenger by simply stamping against his or her name, [1] but this technique was prone to flaws such as vote counting and unjustified results Electronic voting machines were devised to address each of these inequalities. Regardless, the concept of a simple electronic voting system with a disposable memory card was a bit random[2].

We designed an electronic voting machine in Verilog HDL using Xilinx ISE 14.7i that can be implemented on FPGA (Field Programmable Gate Array)[3] hardware

since we realise how difficult it is to manage control signals. Additionally, this execution includes a secret key that is computerised and difficult to hack.

II. LITERATURE SURVEY

The demonstrated in their paper that to overcome these difficulties and build a good electoral method,[4] implementation of electronic mechanical devices in the digital domain is given in this paper. It is difficult to tamper votes in the digital domain and provides a secure and safe technique for conducting elections. May, P., Ehrlich, H.C., and Steinke,[5] In their work, Czajkowski, K., Fitzgerald, S., Foster, I., and Kesselman, C.[6] said that the conventional selection approach was a lengthy and error-prone process.[7] Electronic mechanical device (EVM) polling is a simple, safe,[9] and secure method that takes very little time.[8] Only one vote is accepted by the current Electronic Mechanical Devices (EVMs) used in LOK SABHA and an ASSEMBLY election.[10]

III. PROPOSED METHOD

The Proposed method of electronica voting machine programing is hardware discription language for high rubustness. voting mechanisam that is ahdar based finger printer. traditional paper-based choice technique was a very time-consuming and error-prone process. Electronic mechanical device (EVM) polling is a simple, safe, and secure technology that takes very little time(see figure 1). The suggested digital EVM was created in Verilog HDL and implemented on the FPGA Artix7. The suggested approach has three stages: in the first, we determine the total number of voters and contestants participating in the election process.

Voter can understand easily to elect the member as given adhar based biometric and LCD Displasy shows the symbol of the party to ensure easily identify the which symbole or which party they voting was cast. The process also evvery one understand easily and high rubbestness . Moreover counting process also high speed and more effeicient of data analysis more secure.

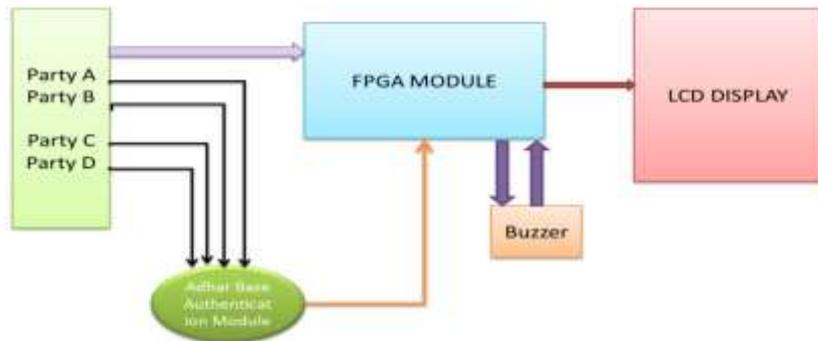


Fig 1. Block diagram of EVM

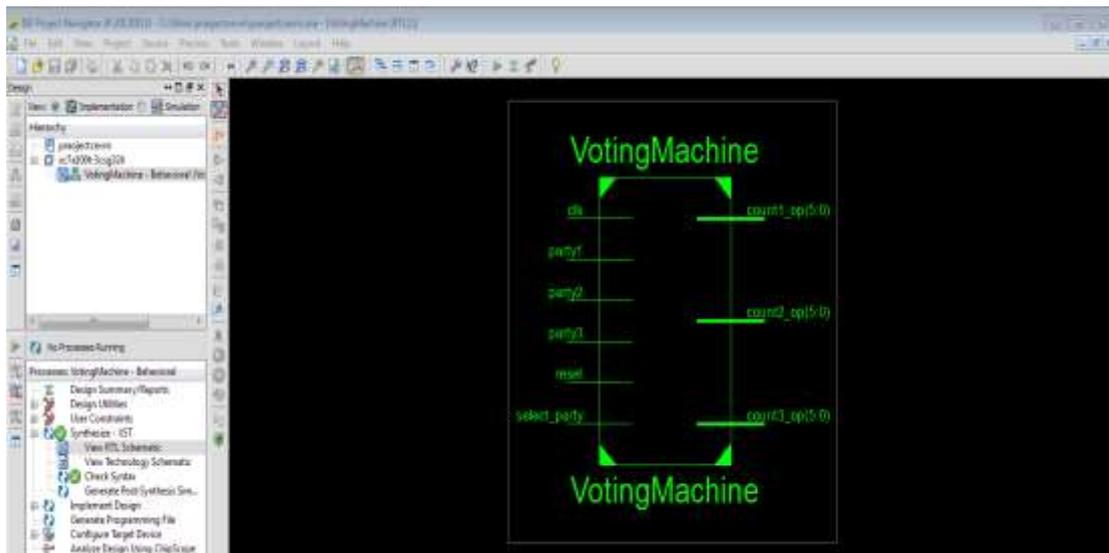


Figure 2: Voting machine schematic diagram

IV. RESULT AND ANALYSIS

The HDL language is implemented on Electronic voting machine schematic, figure 2 shows the number of parties included and no of symbols is there and like inputs and outputs. The schematic figure 3 shows the inputs

voter_switch, clk, voting_en and the outputs (see figure 4 and 5) of the module are party1, party2, party3, reset, select party, output count1(5,0), count2(5,0), count3(5,0)

The screenshot shows a synthesis report for the 'VotingMachine' project. The report is divided into two main sections: 'VotingMachine Project Status' and 'Device Utilization Summary'.

VotingMachine Project Status (05/02/2022 - 09:07:59)			
Project File:	projectname.vhdl	Parser Errors:	No Errors
Module Name:	VotingMachine	Implementation Status:	Synthesized
Target Device:	act100k-3csg104	Errors:	No Errors
Product Version:	ISE 14.7	Warnings:	No Warnings
Design Goal:	Balanced	Routing Results:	
Design Strategy:	Use Default Settings	Timing Constraints:	
Environment:	System Settings	Final Timing Score:	

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	21	12800	0%
Number of Slice LUTs	20	6340	0%
Number of Fully used LUTFF pairs	21	29	72%
Number of bonded IOBs	24	118	13%
Number of BUFGCTRLs	1	32	3%

Figure 3: Synthesis report for hdl program

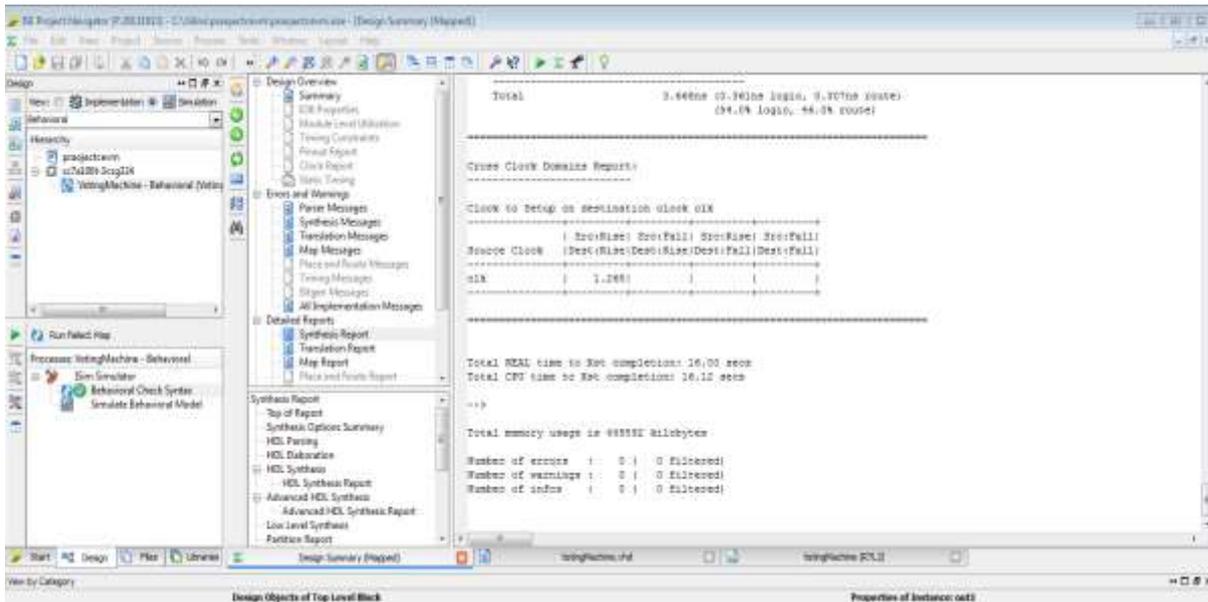


Figure 4: Result and analysis for the clk analysis for the party voting timing cycle

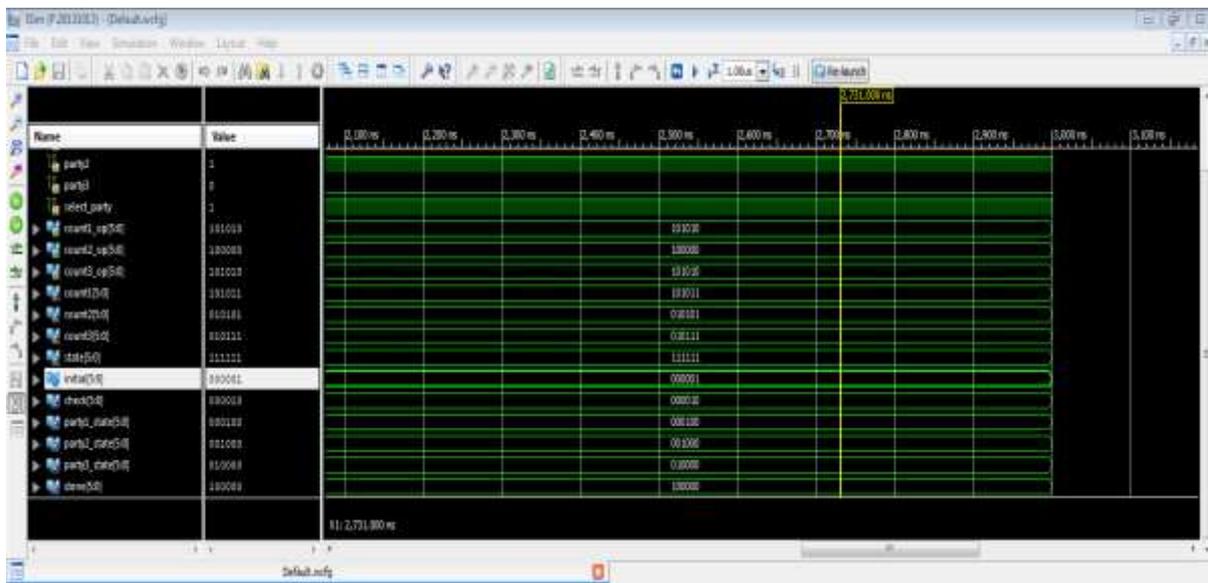


Figure 5: Simulation result for electronic voting mehine using hdl

V. CONCLUSION

The Proposed electronic voting machine designed for a Hardware Discription language using high robustness and exact design and more secure useful fulfilled election standards such as enrolling the entire number of voters and candidates in the first stage, allowing the voter to vote for a specific party of his choice, which is then certified by the opled in the second step. In the final step, it compares all of the legal votes cast for various parties to determine the election winner. We can now say with certainty that the simulated design can be implemented on any FPGA board. It is one of the secure and safe voting mechanisms. Because of Adhar based bio metric is attached with machine to avoid fake voting and rigging, One of the most important aspects of the project is the EVM's security section, where each voter will have his or her own voting card and the password will be his or her

finger print. The voter's identification will be scanned by the computer, and if the voter is confirmed to be eligible, the polling officer will allow them to vote.

CONFLICTS OF INTEREST

The authors declare that they have no conflicts of interest.

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