

Design and Implementation of Data Acquisition System for Low Field MRI Systems

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ABSTRACT

A novel approach of using fully digital radiofrequency (RF) electronics for the design of dedicated Magnetic Resonance Imaging (MRI) systems at low-field (1 mT) is implemented and presented. This digital electronics is based on the use of three key elements: a Direct Digital Synthesizer (DDS) for RF signal generation, a Software Defined Radio (SDR) for digital receiving of MRI signals and a Digital Signal Processor (DSP) for system control and advanced signal processing. The signal generator was developed and implemented using FPGA SPARTAN 3 evaluation board. In addition, basic low pass filters were also designed. The underlying ideas were to enable such low field MRI systems to utilize from existing advanced technology in the telecommunication domain, making them easy to implement and cost effective

Keywords

RF electronics, Magnetic Resonance Imaging, Direct Digital Synthesizer, FPGA, Larmor frequency

1. INTRODUCTION

Magnetic resonance Imaging (MRI) is a powerful, non-invasive standard technique for modern medical care used for detecting abnormalities like cancer, stroke, heart disease, trauma and neurological conditions among other medical tests and imaging systems (Ernst et al, 1998). It is a medical imaging technique which produces high quality soft tissue contrast images of organs inside the human body. MRI is based on the absorption and emission of energy in the radio frequency (RF) range of the electromagnetic spectrum and does not use ionizing radiation unlike CT, X-rays and PET scans.

In a typical experiment, the sample is subjected to a short excitation pulse of radio-frequency (RF) range having magnetic field B_1 , which is applied perpendicularly to the static magnetic field (B_0) at the characteristic Larmor frequency f_0 . This frequency depends on the gyro-magnetic ratio (γ) of the atom and the static main magnetic field according to equation (1):

$$f_0 = \frac{\gamma \cdot B_0}{2\pi} \dots \dots \dots (1)$$

For a proton (^1H nucleus), the Larmor frequency is about 42.49 MHz at $B_0=1\text{T}$ and 42.49 KHz at 1mT.

After synthesis of the RF pulse is fed to a coil which holds the sample via a radio frequency amplifier. The MRI signals (Free Induction Decay) are obtained via the same coil after a delay time. This FID is acquired at the receiving end where the signal is

processed, filtered, amplified and sent to the core processor for further image processing. The final image would be displayed on a monitor as per its design.

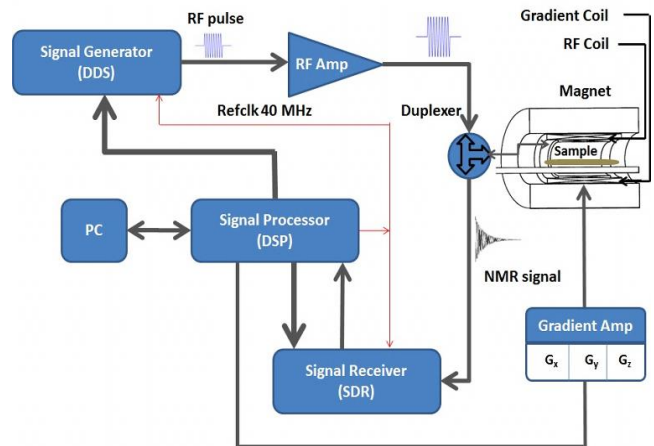


Figure 1: Block diagram of a low field MRI system

A general low field MRI system uses its electronics based on three key elements namely a Direct Digital Synthesizer (DDS) for pulse generation, a Software Defined Radio (SDR) for signal receiving and a Digital Signal Processor (DSP) as a controller. Presently, in this paper we focus on a new design of digital electronics for signal synthesis using FPGA SPARTAN 3 evaluation board. This current technology provides a brief idea about the of hardware and software architecture of the signal generator for a low filed MRI system whose core parameters can be easily updated/extended for a large number of applications and different working frequencies (100 Hz to 77 KHz) with minimum development time and cost.

2. MATERIALS AND METHODS

2.1 Direct Digital Synthesizer

The Direct Digital Synthesizer technology is based on the fact that, a sinusoidal wave with known frequency, amplitude and phase can be synthesized by specifying a set of values (look up table) taken at equal intervals. These series of values are supplied to a Digital-to-Analog Converter (DAC) which intern provides the synthesized analog sine wave signal. Figure 2 shows a simplified block diagram of a fundamental DDS system.

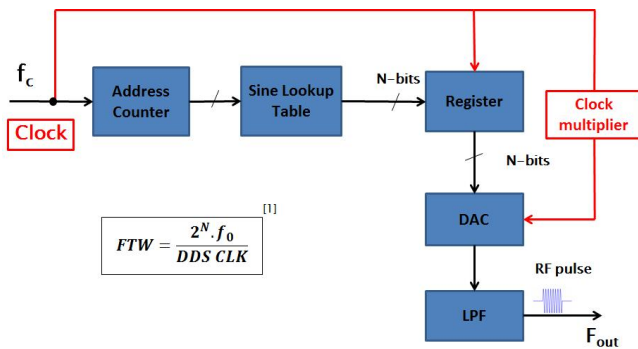


Figure 2: Block diagram of fundamental Direct Digital Synthesis (DDS) system

The heart of the DDS system is the phase accumulator which is depicted as the register block, whose contents are updated once each clock cycle (Figure 2). Each time the phase accumulator is updated, the FTW which is stored in the phase register is added to the phase accumulator register. For an n-bit phase accumulator (range 8 to 48 bits) there are 2^N possible phase points. The truncated output of the phase accumulator serves as the address to a sine (or cosine) lookup table. Each address in the lookup table corresponds to a phase point on the sine wave from 0° to 360° . The lookup table contains 36 data points (can be upgraded from 360 to 1440 data points) with its corresponding digital amplitude information for one complete cycle of a sine wave. The look up table therefore maps the phase information from the phase accumulator into a digital amplitude word, which in turn drives an 8-bit Digital to Analog Converter.

The FTW represents the amount by which the phase accumulator is incremented every clock cycle. The internal architecture of DDS system along with the signal transition is shown in Figure 3.

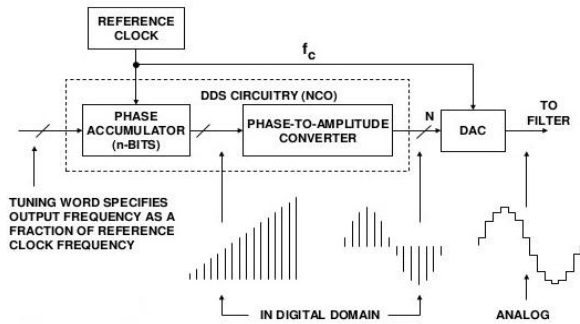


Figure 3: Internal architecture of DDS system showing signal transition

The desired output frequency F_0 is translated to a Frequency Tuning Word (FTW) using equation 2 shown below:

$$FTW = \frac{2^N \cdot f_0}{DDS CLK} \dots\dots (2)$$

Where, N is the frequency resolution (accumulator size in bits), FTW is a decimal number, DDSCLK is the frequency of the DDS clock and frequency f_0 is expressed in Hertz.

3. DISCUSSION

3.1 Testing Using Single Stage (elliptical) Low Pass Filter

A simple low pass filter was constructed using a bread board, resistor and capacitor. The input to this circuit was from the signal generator (DDS) which had $1 V_{p-p}$ as the input signal applied to the circuit. For the purpose of testing the circuit, we considered the capacitance (C) as $0.1 \mu F$, resistance (R) as $1.59 K\Omega$ (through dynamic resistance box) and the cut-off frequency (f_c) at 1 KHz in order to filter the output signal from all the higher frequencies present within it. The input signal to this circuit was taken directly from the output of the signal synthesizer (FPGA) via an 8 bit DAC. Also two finite impulse response filters were created using Filter Design Analysis (FDA) tool in Matlab and desired magnitude response and impulse response of the former were simulated.

4. CONCLUSION

In the proposed design, analog components (DDS) were replaced with digital electronics which facilitated reduction of noise in the system, reduced cost and power consumption compared to conventional 1.5/3/7 Tesla MRI system. The flexibility of the DDS system allowed the user to modify or change parameters without any major hardware and software modification, for a wide variety of MRI applications. The GUI for the low field MRI system is very simple to understand and was created using LabWindows/CVI. The signal synthesis was performed using FPGA board (SPARTAN3 XC3S50) by interfacing it with an 8-bit DAC (NFC-06 Ver.2) and the output was connected to a CRO (30 MHz) through a single stage low pass filter and also FIR filters were designed for the same.

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